

In re: Hans Jurgen Martausch  
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wherein said shared memory is adapted to copy contents of one of said multi-port memories, which has been changed by a writing operation from said user side, to other multi-port memories through said at least one copybus.

#### REMARKS

This Amendment is filed in response to the Final Office Action dated July 19, 2002. Applicant first notes with appreciation the Examiner's thorough examination of the application as evidenced by the Office Action. In response to the Office Action, Applicant has amended independent Claim 1 to more clearly define the claimed invention. As discussed in detail below, Applicant respectfully submits that amended independent Claim 1, as well as the claims that depend therefrom, includes recitations that patentably define over the cited references, taken either individually or in combination. In light of this, Applicant respectfully requests reconsideration and allowance of the application.

The Office Action has again rejected all of the pending claims of the application as either anticipated by U.S. Patent No. 6,321,298 to Hubis or obvious in light of the Hubis '298 patent in combination with either U.S. Patent No. 6,223,260 to Gujral et al. or U.S. Patent No. 6,021,472 to Hamaguchi.

With regard to Figure 3 of the Hubis '298 patent, the Office Action alleges that the controllers 104 and the memories 202 located therein constitute shared memories. The Office Action alleges that bus 110 acts as a copy bus, and because each controller 104 has an independent connection to the host 102, the arrangement of the Hubis '298 patent is a shared memory anticipating the claimed invention. Applicant, however, disagrees with this assessment of the prior art.

The memory configuration of the Hubis '298 patent pointed to by the Office Action is not a share memory, as recited in amended independent Claim 1. A shared memory is defined in the art as a memory capable of supplying an identical database to several users, i.e., sharing the possibility of read and write accesses to identical data by all users. The memories 202 for each controller 104 of the Hubis '298 patent do not supply identical

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databases for several users. Instead, each of these memories only include data that has been altered, they do not contain an entire record of all data. In fact, the Hubis '298 patent requires the memories 202 of each controller 104 in combination with the memory devices 108 to create a shared memory. Because, the memories 202 for each controller 104 do not include a complete copy of all data and thus are not a share memory, the controllers themselves cannot be seen as meeting the plurality of memories as recited in amended independent Claim 1. Instead, for the Hubis '298 patent to arguably meet the claimed invention, each controller 104 in combination with the shared memory 108 must be compared to amended independent Claim 1. In this instance, the system of the Hubis '298 patent does not teach or suggest the claimed invention.

This configuration does not allow for internally concurrent accesses to the memory as recited in amended independent Claim 1. Specifically, the share memory 108 does not have at least two access ports for concurrent access, instead only one common port is connected to all controllers 104. Specifically, as shown in Figure 3, there is only one bus 110 between the memory 108 and the controllers 104 not at least two ports, as recited in amended independent Claim 1. Further, the internal memory 108 is connected via the bus 110 to each of the controllers 104. This connection is used for both copying data and for accessing data. As such, the system of the Hubis '298 patent does not teach or suggest a copy bus that is independent of at least two access ports, as recited in amended independent Claim 1. This is a very important distinction and accounts for a major operating difference between the memory of the claimed invention and that of the Hubis '298 patent.

Specifically, because there is only one access bus 110 connected between the controllers 104 and the memory 108, there cannot be concurrent accesses to the memory in the Hubis '298 patent. In the Hubis '298 patent, if the host computer 102 requests data from a controller 104 that is not located in the controller's memory 202, the controller must access the memory 108 via the bus 112. This action blocks all of the other controllers 104 from

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using the bus 112. As such, concurrent access of the memory, as recited in amended independent Claim 1, is not possible using the system of the Hubis '298 patent.

As mentioned previously and reiterated here, the combination of the Gujral '260 and Hamaguchi '472 patents with the Hubis '296 patent does not teach or suggest a shared memory having true multi-port memories. Specifically, the Gujral '260 and Hamaguchi '472 patents do not disclose true multi-port memories. Instead, they disclose only pseudo multi-port memories. They include controllers, (which a true multi-port memory would not have), to turn concurrent reads of the two ports into sequential reads. As such, the pseudo multi-port memories support k concurrent accesses to an N port memory, while the true multi-port memory of the claimed invention provides N concurrent accesses to N ports.

In light of the above, Applicant respectfully submits that none of the cited references, taken either individually or in combination, teaches or suggests a shared memory having true multi-port memories as recited in amended independent Claim 1. As such, Applicant respectfully submits that amended independent Claim 1, as well as the claims that depend therefrom, is patentable over the cited references.

### CONCLUSION

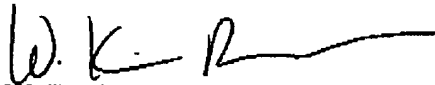
In view of the amended claim and the remarks presented above, it is respectfully submitted that all of the present claims of the application are in condition for immediate allowance. It is therefore respectfully requested that a Notice of Allowance be issued. The Examiner is encouraged to contact Applicant's undersigned attorney to resolve any remaining issues in order to expedite examination of the present application.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those, which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a),

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and any fee required therefore (including fees for net addition of claims) is hereby authorized to be charged to Deposit Account No. 16-0605.

Respectfully submitted,



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CERTIFICATION OF FACSIMILE TRANSMISSION	CERTIFICATE OF MAILING
<p>I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office at Fax No. 703-746-7138 on the date shown below.</p> <p><u>Elaine Kelly</u> (Type or print name of person signing certification.)</p> <p> <u>10-21-02</u> Signature Date</p>	<p>I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: BOX AF, Commissioner for Patents, Washington, DC 20231, on October 21, 2002.</p> <p>_____</p>

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**Version with Markings to Show Changes Made:**

**In the Claims:**

Please amend Claim 1 as follows:

1. (Twice Amended) A shared memory comprising:

a plurality of true multi-port memories, wherein each memory has at least two access ports accessible from a user side, wherein said at least two access ports allow for internally concurrent access to data stored in the memory [having N independent ports that allow internal concurrent accesses of the memory for all N port], wherein each memory further has at least one port with a copybus-function separate from said at least two access ports [, and at least one port accessible from user side]; and

at least one copybus connected to each of said at least one ports having the copybus-function;

wherein said shared memory is adapted to copy contents of one of said multi-port memories, which has been changed by a writing operation from said user side, to other multi-port memories through said at least one copybus.

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